SCHOTTKY BIPOLAR LSI MICROCOMPUTER SET

3002 CENTRAL PROCESSING ELEMENT

The INTEL Bipolar Microcomputer Set is a family of Schottky bipolar LSI circuits which simplify the construction of microprogrammed central processors and device controllers. These processors and controllers are truly microprogrammed in the sense that their control logic is organized around a separate read-only memory called the microprogram memory. Control signals for the various processing elements are generated by the microinstructions contained in the microprogram memory. In the implementation of a typical central processor, as shown below, the microprogram interprets a higher level of instructions called macroinstructions, similar to those found in a small computer. For device controllers, the microprograms directly implement the required control functions.

The INTEL 3002 Central Processing Element contains all of the circuits that represent a 2-bit wide slice through the data processing section of a digital computer. To construct a complete central processor for a given word width N, it is simply necessary to connect an array of N/2 CPE's together. When wired together in such an array, a set of CPE's provide the following capabilities:

- 2's complement arithmetic
- Logical AND, OR, NOT and exclusive-OR
- Incrementing and decrementing
- Shifting left or right
- Bit testing and zero detection
- Carry look-ahead generation
- Multiple data and address busses

High Performance — 100 ns Cycle Time

TTL and DTL Compatible

N-Bit Word Expandable Multi-Bus Organization
- **3 Input Data Busses**
- **2 Three-State Fully Buffered Output Data Busses**

11 General Purpose Registers

Full Function Accumulator

Independent Memory Address Register

Cascade Outputs for Full Carry Look-Ahead

Versatile Functional Capability
- **8 Function Groups**
- **Over 40 Useful Functions**
- **Zero Detect and Bit Test**

Single Clock

28 Pin DIP

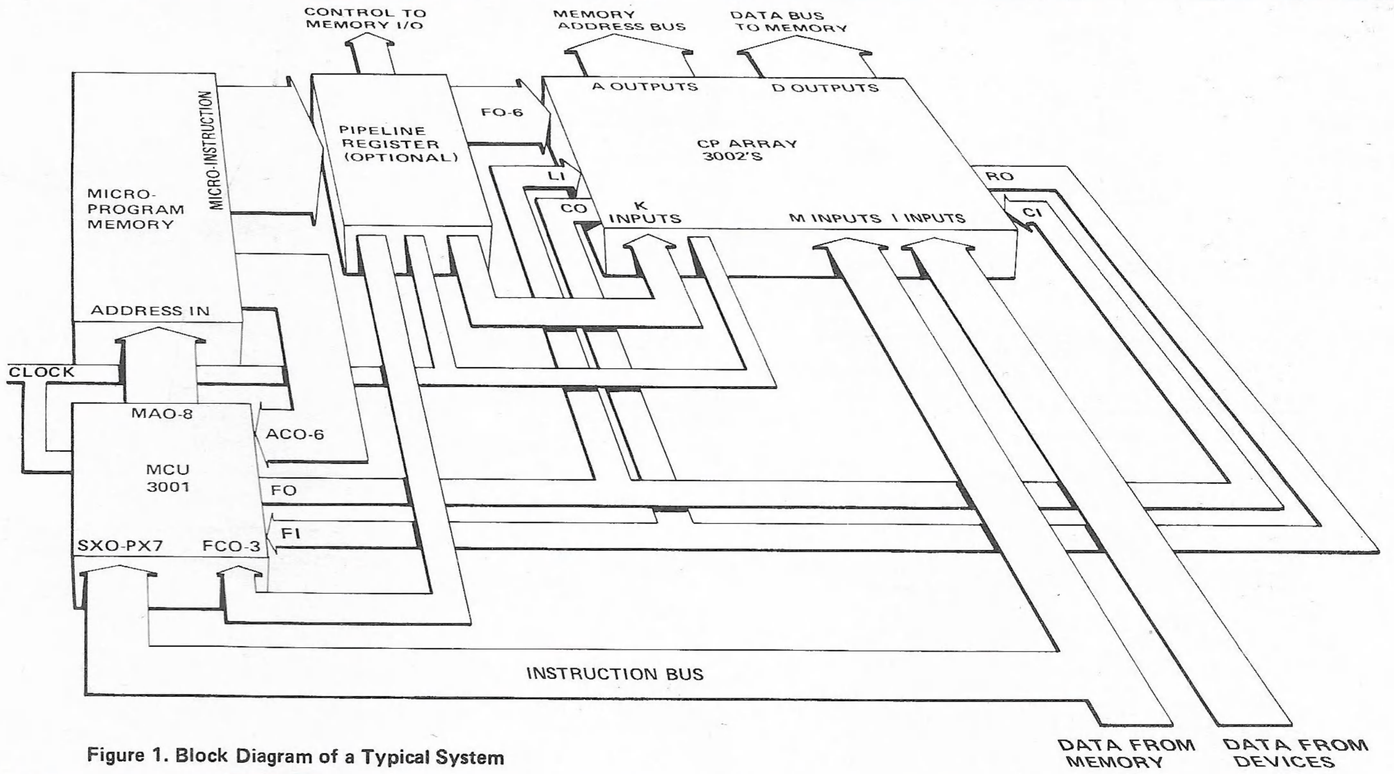

Figure 1. Block Diagram of a Typical System

Other members of the INTEL Bipolar Microcomputer Set:

3001	Microprogram Control Unit
3003	Look-Ahead Carry Generator
3212	Multi-Mode Latch Buffer
3214	Priority Interrupt Control Unit
3226	Inverting Bi-Directional Bus Driver
3301	Schottky Bipolar ROM (256 x 4)
3304A	Schottky Bipolar ROM (512 x 8)
3601	Schottky Bipolar PROM (256 x 4)
3604	Schottky Bipolar PROM (512 x 8)

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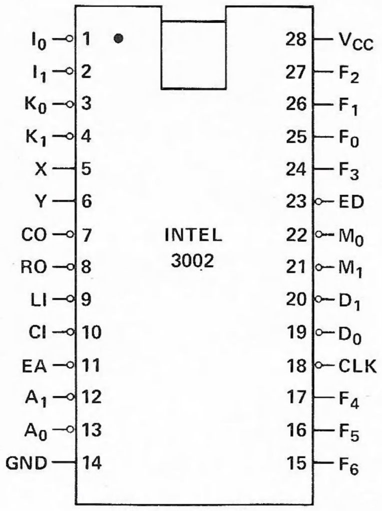
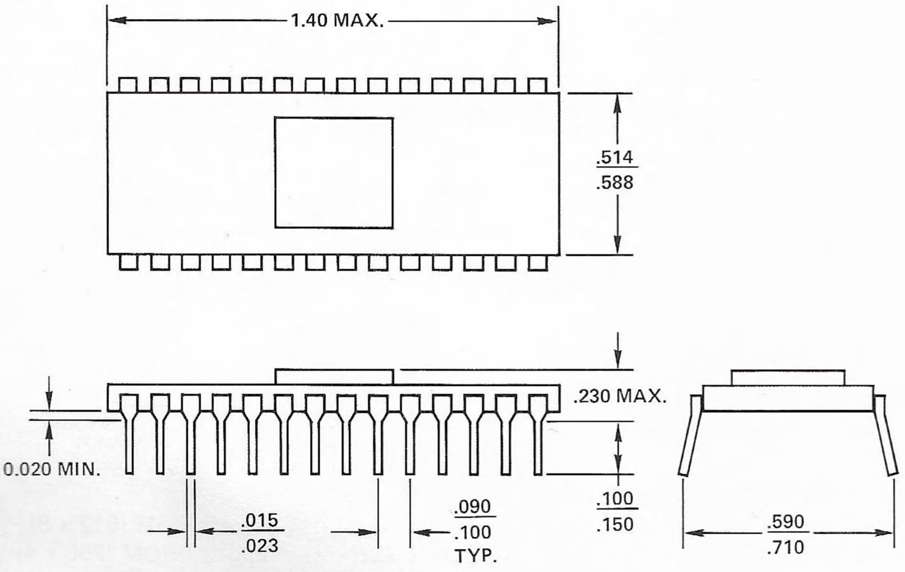
PACKAGE CONFIGURATION



PACKAGE OUTLINE



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1, 2	I_0-I_1	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active LOW
3, 4	K_0-K_1	Mask Bus Inputs The mask bus inputs provide a separate input port for the microprogram memory, to allow mask or constant entry.	Active LOW
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the INTEL 3003 Look-Ahead Carry Generator.	
7	CO	Ripply Carry Output The ripple carry output is only disabled during shift right operations.	Active LOW Three-state
8	RO	Shift Right Output The shift right output is only enabled during shift right operations.	Active LOW Three-state
9	LI	Shift Right Input	Active LOW
10	CI	Carry Input	Active LOW
11	EA	Memory Address Enable Input When in the LOW state, the memory address enable input enables the memory address outputs (A_0-A_1).	Active LOW
12-13	A_0-A_1	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active LOW Three-state
14	GND	Ground	
15-17, 24-27,	F_0-F_6	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	
18	CLK	Clock Input	
19-20	D_0-D_1	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active LOW Three-state
21-22	M_0-M_1	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active LOW
23	ED	Memory Data Enable Input When in the LOW state, the memory data enable input enables the memory data outputs (D_0-D_1)	Active LOW
28	V_{CC}	+5 Volt Supply	

NOTE:

[1] Active HIGH, unless otherwise specified.

LOGICAL DESCRIPTION

The CPE provides the arithmetic, logic and register functions of a 2-bit wide slice through a microprogrammed central processor. Data from external sources such as main memory, is brought into the CPE on one of the three separate input busses. Data being sent out of the CPE to external devices is carried on either of the two output busses. Within the CPE, data is stored in one of eleven scratchpad registers or in the accumulator. Data from the input busses, the registers, or the accumulator is available to the arithmetic/logic section (ALS) under the control of two internal multiplexers. Additional inputs and outputs are included for carry propagation, shifting, and micro-function selection. The complete logical organization of the CPE is shown below.

MICRO-FUNCTION BUS AND DECODER

The seven micro-function bus input lines of the CPE, designated F_0–F_6, are decoded internally to select the ALS function, generate the scratchpad address, and control the A and B multiplexers.

M-BUS AND I-BUS INPUTS

The M-bus inputs are arranged to bring data from an external main memory into the CPE. Data on the M-bus is multiplexed internally for input to the ALS.

The I-bus inputs are arranged to bring data from an external I/O system into the CPE. Data on the I-bus is also multiplexed internally, although independently of the M-bus, for input to the ALS Separation of the two busses permits a relatively lightly loaded memory bus even though a large number of I/O devices are connected to the I-bus. Alternatively, the I-bus may be wired to perform a multiple bit shift (e.g., a byte exchange) by connecting it to one of the output busses. In this case, I/O device data is gated externally onto the M-bus.

SCRATCHPAD

The scratchpad contains eleven registers designated R_0 through R_9 and T. The output of the scratchpad is multiplexed internally for input to ALS. The ALS output is returned for input into the scratchpad.

ACCUMULATOR AND D-BUS

An independent register called the accumulator (AC) is available for storing the result of an ALS operation. The output of the accumulator is multiplexed internally for input back to the ALS and is also available via a three-state output buffer on the D-bus outputs. Conventional usage of the D-bus is for data being sent to the external main memory or to external I/O devices.

A AND B MULTIPLEXERS

The A and B multiplexers select the two inputs to the ALS specified on the micro-function bus. Inputs to the A-multiplexer include the M-bus, the scratchpad, and the accumulator. The B-multiplexer selects either the I-bus, the accumulator, or the K-bus. The selected B-multiplexer input is always logically ANDed with the data on the K-bus (see below) to provide a flexible masking and bit testing capability.

ALS AND K-BUS

The ALS is capable of a variety of arithmetic and logic operations, including 2's complement addition, incrementing, and decrementing, plus logical AND, inclusive-OR, exclusive-NOR, and logical complement. The result of an ALS operation may be stored in the accumulator or one of the scratchpad registers. Separate left input and right output lines, designated LI and RO, are available for use in right shift operations. Carry input and carry output lines, designated CI and CO are provided for normal ripple carry propagation. CO and RO data are brought out via two alternately enabled tri-state buffers. In addition, standard look ahead carry outputs, designated X and Y, are available for full carry look ahead across any word length.

The ability of the K-bus to mask inputs to the ALS greatly increases the versatility of the CPE. During non-arithmetic operations in which carry propagation has no meaning, the carry circuits are used to perform a word-wise inclusive-OR of the bits, masked by the K-bus, from the register or bus selected by the function decoder. Thus, the CPE provides a flexible bit testing capability. The K-bus is also used during arithmetic operations to mask portions of the field being operated upon. An additional function of the K-bus is that of supplying constants to the CPE from the microprogram.

MEMORY ADDRESS REGISTER AND A-BUS

A separate ALS output is also available to the memory address register (MAR) and to the A-bus via a three-state output buffer. Conventional usage of the MAR and A-bus is for sending addresses to an external main memory. The MAR and A-bus may also be used to select an external device when executing I/O operations.

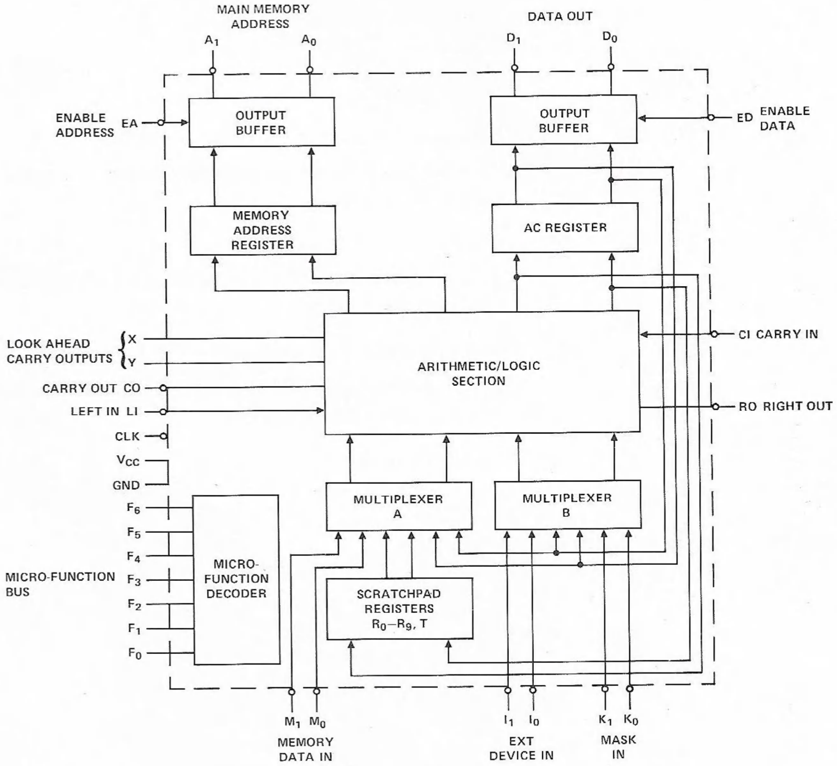


Figure 2. 3002 Block Diagram

During each micro-cycle, a micro-function is applied to F-bus inputs of the CPE. The micro-function is decoded, the operands are selected by the multiplexers, and the specified operation is performed by ALS. If a negative going clock edge is applied, the result of the ALS operation is either deposited in the accumulator or written into the selected scratchpad register. In addition, certain operations permit related address data to be deposited in the MAR. A new micro-function should only be applied following the rising edge of the clock.

By externally gating the clock input to CPE, referred to as conditional clocking, the clock pulse may be selectively omitted during a micro-cycle. Since the carry, shift, and look-ahead circuits are not clocked, their outputs may be used to perform a variety of non-destructive tests on data in the accumulator or in the scratchpad. No register contents are modified by the operation due to the absence of the clock pulse.

The micro-function to be performed is determined from the function group (F-Group) and register group (R-Group) selected by the data on the F-bus. The F-Group is specified by the upper three bits of data, F_4-F_6. The R-Group is specified by the lower four bits of data, F_0-F_3. R-Group I contains R_0 through R_9, T, and AC and is denoted by the symbol R_n. R-Group II and R-Group III contain only T and AC. F-Group and R-Group formats are summarized in Appendix A.

The following is a detailed explanation of each of the CPE micro-functions. A general functional description of each operation is given followed by two additional descriptions which explain the result of the micro-function with both K-bus inputs at logical 0 or both at logical 1. In most cases, the effect of placing the K-bus in the all-one or the all-zero state is to either select or deselect the accumulator in the operation, respectively. A micro-function mnemonic is included with each description for reference purposes and to assist in the design of micro-assembly languages. The micro-functions are summarized in Appendix B. The effective micro-functions for the all-zero and the all-one K-bus states are summarized in Appendix C and D, respectively.

F-GROUP 0 R-GROUP I

Logically AND the contents of AC with the data on the K-bus. Add the result to the contents of R_n and the value of the carry input (CI). Deposit the sum in AC and R_n.

ILR K-BUS = 00

Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the result in AC.

ALR K-BUS= 11

Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.

F-GROUP 0 R-GROUP II

Logically AND the contents of AC with the data on the K-bus. Add the result to CI and the data on the M-bus. Deposit the sum in AC or T, as specified.

ACM K-BUS = 00

Add CI to the data on the M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.

AMA K-BUS = 11

Add the data on the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.

F-GROUP 0 R-GROUP III

(General description omitted, see Appendix B.)

SRA K-BUS = 00

Shift the contents of AC or T, as specified, right one bit position. Place the previous low order bit value on RO and fill the high order bit from the data on LI. Used to shift or rotate AC or T right one bit.

(K-bus = 11 description omitted, see Appendix B.)

F-GROUP 1 R-GROUP I

Logically OR the contents of R_n with the data on the K-bus. Deposit the result in MAR. Add the data on the K-bus to contents of R_n and CI. Deposit the result in R_n.

LMI K-BUS = 00

Load MAR from R_n. Conditionally increment R_n. Used to maintain a macro-instruction program counter.

DSM K-BUS = 11

Set MAR to all one's. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement R_n.

F-GROUP 1 R-GROUP II

Logically OR the data on the M-bus with the data on the K-bus. Deposit the result in MAR. Add the data on the K-bus to the data on the M-bus and CI. Deposit the sum in AC or T, as specified.

LMM K-BUS = 00

Load MAR from the M-bus. Add CI to the data on the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.

LDM K-BUS = 11

Set MAR to all ones. Subtract one from the data on the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.

F-GROUP 1 R-GROUP III

Logically OR the data on the K-bus with the complement of the contents of AC or T, as specified. Add the result to the logical AND of the contents of specified register with the data on the K-bus. Add the sum to CI. Deposit the result in the specified register.

CIA K-BUS = 00

Add CI to the complement of the contents of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.

DCA K-BUS = 11

Subtract one from the contents of AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.

F-GROUP 2 R-GROUP I

Logically AND the data on the K-bus with the contents of AC. Subtract one from the result and add the difference to CI. Deposit the sum in R_n.

CSR K-BUS = 00

Subtract one from CI and deposit the difference in R_n. Used to conditionally clear or set R_n to all 0's or 1's, respectively.

SDR K-BUS = 11

Subtract one from AC and add the difference to CI. Deposit the sum in R_n. Used to store AC in R_n or to store the decremented value of AC in R_n.

F-GROUP 2 R-GROUP II

Logically AND the data on the K-bus with the contents of AC. Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.

CSA K-BUS = 00

Subtract one from CI and deposit the difference in AC or T, as specified. Used to conditionally clear or set AC or T.

SDA K-BUS = 11

Subtract one from AC and add the difference to CI. Deposit the sum in AC or T, as specified. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.

F-GROUP 2 R-GROUP III

Logically AND the data of the K-bus with the data on the I-bus. Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.

(K-bus = 00 description omitted, see CSA above.)

LDI K-BUS = 11

Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified.
Used to load input bus data or decremented input bus data in the specified register.

F-GROUP 3 R-GROUP I

Logically AND the contents of AC with the data on the K-bus. Add the contents of R_n and CI to the result. Deposit the sum in R_n.

INR K-BUS = 00

Add CI to the contents of R_n and deposit the sum in R_n. Used to increment R_n.

ADR K-BUS = 11

Add the contents of AC to R_n. Add the result to CI and deposit the sum in R_n. Used to add the accumulator to a register or to add the incremented value of the accumulator to a register.

F-GROUP 3 R-GROUP II

(All descriptions omitted, identical to F-Group 0/R-Group II described above.)

F-GROUP 3 R-GROUP III

Logically AND the data on the K-bus with the data on the I-bus. Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.

INA K-BUS = 00

Conditionally increment the contents of AC or T, as specified. Used to increment AC or T.

AIA K-BUS = 11

Add the data on the I-bus to the contents of AC or T, as specified. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.

F-GROUP 4 R-GROUP I

Logically AND the data on the K-bus with the contents of AC. Logically AND the result with the contents of R_n. Deposit the final result in R_n. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.

CLR K-BUS = 00

Clear R_n to all 0's. Force CO to CI. Used to clear a register and force CO to CI.

ANR K-BUS = 11

Logically AND AC with R_n. Deposit the result in R_n. Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.

F-GROUP 4 R-GROUP II

Logically AND the data on the K-bus with the contents of AC. Logically AND the result with the data on the M-bus. Deposit the final result in AC or T, as specified. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry.OR on CO.

CLA K-BUS = 00

Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.

ANM K-BUS = 11

Logically AND the data on the M-bus with the contents of AC. Deposit the result in AC or T, as specified. Force CO to one if the result is non-zero. Used to AND M-bus data to the accumulator and test for a zero result.

F-GROUP 4 R-GROUP III

Logically AND the data on I-bus with the data on the K-bus. Logically AND the result with the contents of AC or T, as specified. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.

(K-bus = 00 description omitted, see CLA above.)

ANI K-BUS = 11

Logically AND the data on the I-bus with the contents of AC or T, as specified. Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.

F-GROUP 5 R-GROUP I

Logically AND the data on the K-bus with the contents of R_n. Deposit the result in R_n. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.

(K-bus = 00 description omitted, see CLR above.)

TZR K-BUS = 11

Force CO to one if R_n is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register (see general description) for masking and, optionally, testing for a zero result.

F-GROUP 5 R-GROUP II

Logically AND the data on the K-bus with the data on the M-bus. Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.

(K-bus = 00 description omitted, see CLA above.)

LTM K-BUS = 11

Load AC or T, as specified, with data from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for a zero result. Also used to AND K-bus data with M-bus data (see general description) for masking and, optionally, testing for a zero result.

F-GROUP 5 R-GROUP III

Logically AND the data on K-bus with contents of AC or T, as specified. Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.

(K-bus = 00 description omitted, see CLA above.)

TZA K-BUS = 11

Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND K-bus data to the specified register (see general description) for masking and, optionally, testing for a zero result.

F-GROUP 6 R-GROUP I

Logically OR CI with the word-wise OR of the logical AND of AC and the data on the K-bus. Place the result of the carry OR on CO. Logically OR the contents of R_n with the logical AND of AC and the data on the K-bus. Deposit the result in R_n.

NOP K-BUS = 00

Force CO to CI. Used as a null operation or to force CO to CI.

ORR K-BUS = 11

Force CO to one if AC is non-zero. Logically OR the contents of the accumulator to the contents of R_n. Deposit the result in R_n. Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.

F-GROUP 6 R-GROUP II

Logically OR CI with the word-wise OR of the logical AND of AC and the data on the K-bus. Place the value of the carry OR on CO. Logically OR the data on the M-bus, with the logical AND of AC and the data on the K-bus. Deposit the final result in AC or T, as specified.

LMF K-BUS = 00

Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to CI.

ORM K-BUS = 11

Force CO to one if AC is non-zero. Logically OR the data on the M-bus with the contents of AC. Deposit the result in AC or T, as specified. Used to OR memory data with the accumulator and, optionally, test the previous value of the accumulator for zero.

F-GROUP 6 R-GROUP III

Logically OR CI with the word-wise OR of the logical AND of the data on the I-bus and the data on the K-bus. Place the value of the carry OR on CO. Logically AND the data on the K-bus with the data on the I-bus. Logically OR the result with the contents of AC or T, as specified. Deposit the final result in the specified register.

(K-bus = 00 description omitted, see NOP above.)

ORI K-BUS = 11

Force CO to one if the data on the I-bus is non-zero. Logically OR the data on the I-bus to the contents of AC or T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.

F-GROUP 7 R-GROUP I

Logically OR CI with the word-wise OR of the logical AND of the contents of R_n and AC and the data on the K-bus. Place the value of the carry OR on CO. Logically AND the data on the K-bus with the contents of AC. Exclusive-NOR the result with the contents of R_n. Deposit the final result in R_n.

CMR K-BUS = 00

Complement the contents of R_n. Force CO to CI.

XNR K-BUS = 11

Force CO to one if the logical AND of AC and R_n is non-zero. Exclusive-NOR the contents of AC with the contents of R_n. Deposit the result in R_n. Used to exclusive-NOR the accumulator with a register.

F-GROUP 7 R-GROUP II

Logically OR CI with the word-wise OR of the logical AND of the contents of AC and the data on the K-bus and M-bus. Place the value of the carry OR on CO. Logically AND the data on the K-bus with the contents of AC. Exclusive-NOR the result with the data on the M-bus. Deposit the final result in AC or T, as specified.

LCM K–BUS = 00

Load the complement of the data on the M-bus into AC or T, as specified. Force CO to CI.

XNM K-BUS = 11

Force CO to one if the logical AND of AC and the M-bus data is non-zero. Exclusive-NOR the contents of AC with the data on the M-bus. Deposit the result in AC or T, as specified. Used to exclusive–NOR memory data with the accumulator.

F-GROUP 7 R-GROUP III

Logically OR CI with the word-wise OR of the logical AND of the contents of the specified register and the data on the I-bus and K-bus. Place the value of the carry OR on CO. Logically AND the data on the K-bus with the data on the I-bus. Exclusive-NOR the result with the contents of AC or T, as specified. Deposit the final result in the specified register.

CMA K-BUS = 00

Complement AC or T, as specified. Force CO to CI.

XNI K-BUS = 11

Force CO to one if the logical AND of the specified register and the I-bus data is non-zero. Exclusive-NOR the contents of AC with the data on the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to +5.5V
Output Currents	100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

T_A = 0°C to +70°C

			LIMITS			
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		−0.8	−1.0	V	V_{CC} = 4.75V, I_C = −5 mA
I_F	Input Load Current: F_0–F_6, CLK, K_0, K_1, EA, ED I_0, I_1, M_0, M_1, LI CI		 −0.05 −0.85 −2.3	 −0.25 −1.5 −4.0	 mA mA mA	 V_{CC} = 5.25V, V_F = 0.45V
I_R	Input Leakage Current: F_0–F_6, CLK, K_0, K_1, EA, ED I_0, I_1, M_0, M_1, LI CI			 40 60 180	 μA μA μA	 V_{CC} = 5.25V, V_R = 5.25V
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current		145	190	mA	V_{CC} = 5.25V[2]
V_{OL}	Output Low Voltage (All Output Pins)		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 10 mA
V_{OH}	Output High Voltage (All Output Pins)	2.4	3.0		V	V_{CC} = 4.75V, I_{OH} = −1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	−15	−25	−60	mA	V_{CC} = 5.0V
$I_{O(off)}$	Off State Output Current A_0, A_1, D_0 and D_1 Only			−100 100	μA μA	V_{CC} = 5.25V, V_O = 0.45V V_{CC} = 5.25V, V_O = 5.25V

NOTES:

[1] Typical values are for T_A = 25°C and nominal supply voltage

[2] CLK input grounded, other inputs open.

A.C. CHARACTERISTICS AND WAVEFORMS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%

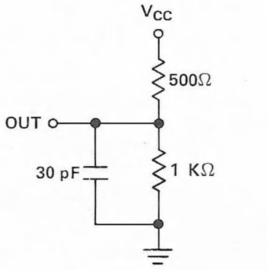
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT
t_{CY}	Clock Cycle Time	100	70		ns
t_{WP}	Clock Pulse Width	33	20		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	60	40		ns
	Data Set-Up Time:				
t_{DS}	I_0, I_1, M_0, M_1, K_0, K_1	50	30		ns
t_{SS}	LI, CI	27	13		ns
	Data and Function Hold Time:				
t_{FH}	F_0 through F_6	5	2		ns
t_{DH}	I_0, I_1, M_0, M_1, K_0, K_1	5	4		ns
t_{SH}	LI, CI	15	2		ns
	Propagation Delay to X, Y, RO from:				
t_{XF}	Any Function Input		37	52	ns
t_{XD}	Any Data Input		29	42	ns
t_{XT}	Trailing Edge of CLK		40	60	ns
t_{XL}	Leading Edge of CLK	17		92	ns
	Propagation Delay to CO from:				
t_{CL}	Leading Edge of CLK	20		105	ns
t_{CT}	Trailing Edge of CLK		48	70	ns
t_{CF}	Any Function Input		43	65	ns
t_{CD}	Any Data Input		30	55	ns
t_{CC}	CI (Ripple Carry)		14	25	ns
	Propagation Delay to A_0, A_1, D_0, D_1 from:				
t_{DL}	Leading Edge of CLK		32	50	ns
t_{DE}	Enable Input ED, EA		12	25	ns

NOTE:
[1] Typical values are for T_A = 25°C and nominal supply voltage.

TEST CONDITIONS:

Input pulse amplitude: 2.5 V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 10 mA and 30 pF.
Speed measurements are made at 1.5 volt levels.

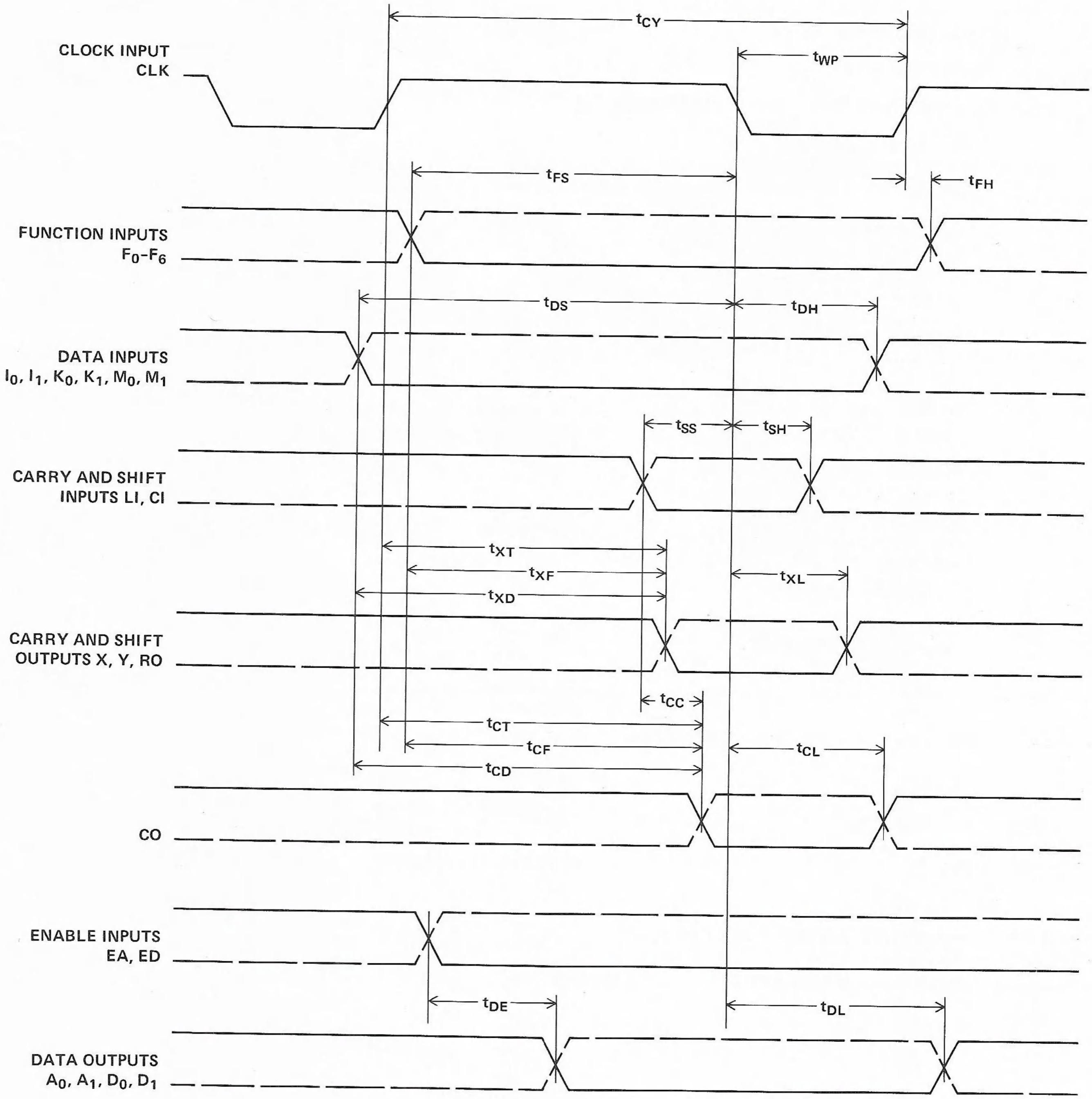
TEST LOAD CIRCUIT:



CAPACITANCE[2] T_A = 25°C

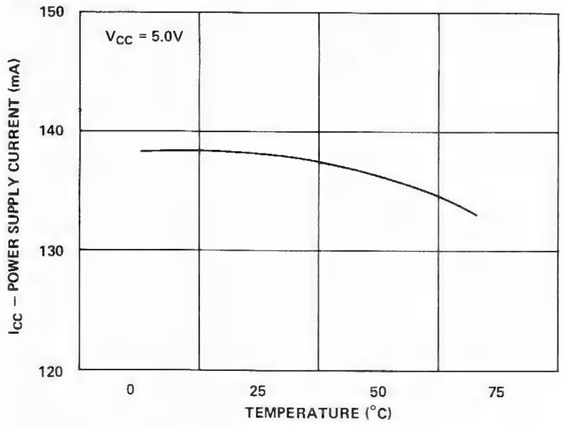
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:
[2] This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V and T_A = 25°C.

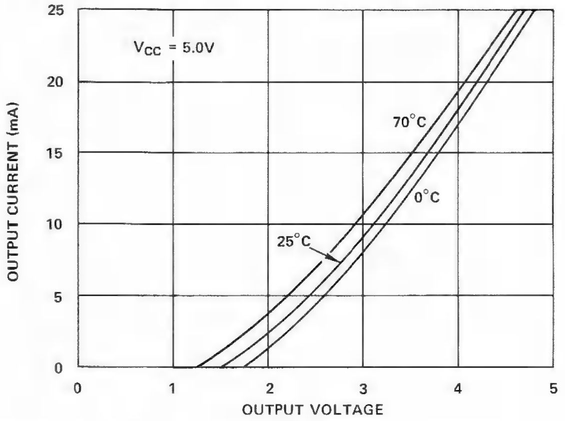

CLOCK INPUT CLK
FUNCTION INPUTS F_0-F_6
DATA INPUTS $I_0, I_1, K_0, K_1, M_0, M_1$
CARRY AND SHIFT INPUTS LI, CI
CARRY AND SHIFT OUTPUTS X, Y, RO
CO
ENABLE INPUTS EA, ED
DATA OUTPUTS A_0, A_1, D_0, D_1
t_{CY}
t_{WP}
t_{FS}
t_{FH}
t_{DS}
t_{DH}
t_{SS}
t_{SH}
t_{XT}
t_{XF}
t_{XD}
t_{XL}
t_{CC}
t_{CT}
t_{CF}
t_{CD}
t_{CL}
t_{DE}
t_{DL}

TYPICAL AC AND DC CHARACTERISTICS

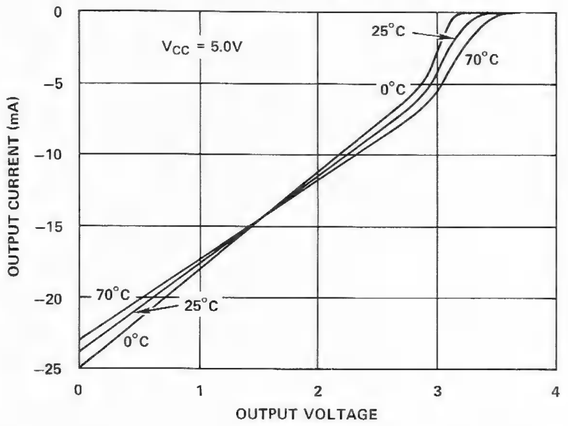
Power Supply Current vs Temperature



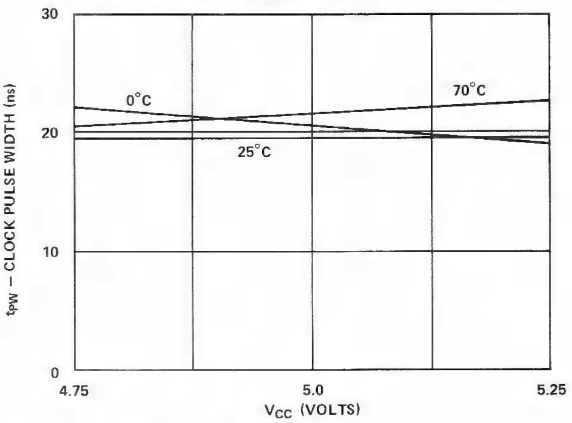
Output Current vs Output Low Voltage



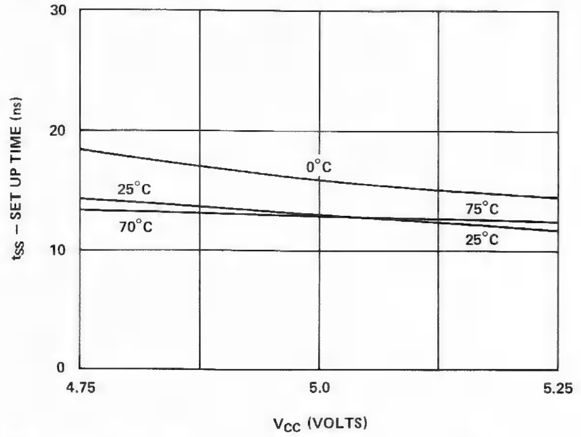
Output Current vs Output High Voltage



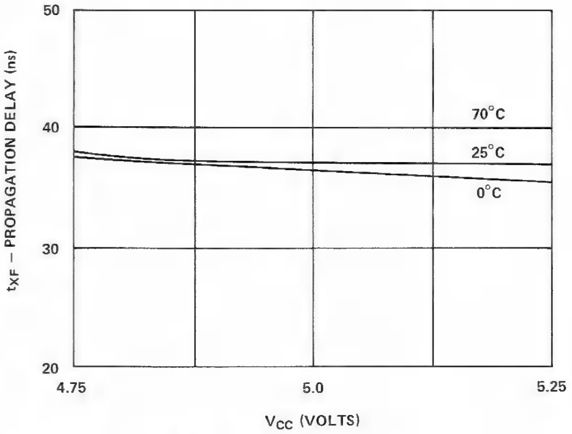
Clock Pulse Width vs V_{CC} and Temperature



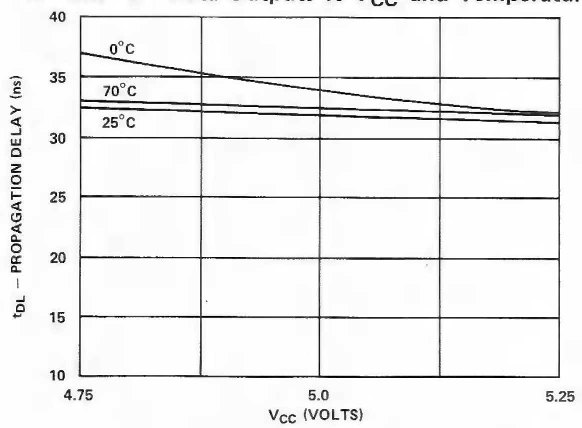
Carry in Set Up Time vs V_{CC} and Temperature



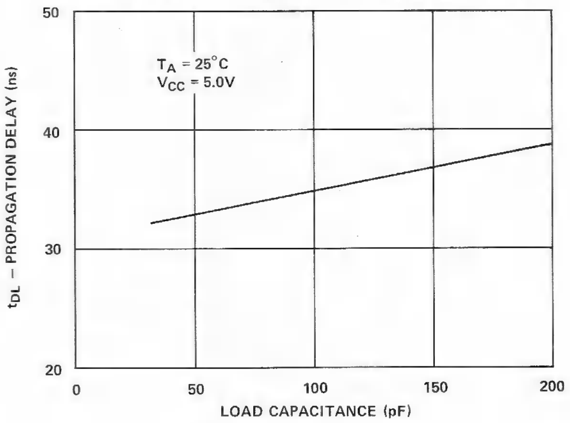
Propagation Delay Function Inputs to Cascade Outputs vs V_{CC} and Temperature



Propagation Delay Clock to "A" and "D" Data Outputs vs V_{CC} and Temperature



Propagation Delay Clock to "A" and "D" Data Output vs Load Capacitance



FUNCTION AND REGISTER GROUP FORMATS

FUNCTION GROUP	F_6	5	4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GROUP	REGISTER	F_3	2	1	0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

APPENDIX B MICRO-FUNCTION SUMMARY

F-GROUP	R-GROUP	MICRO-FUNCTION	
0	I	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	
	II	$M + (AC \wedge K) + CI \rightarrow AT$	
	III	$AT_L \wedge (\overline{I_L \wedge K_L}) \rightarrow RO$ $[AT_L \wedge (I_L \wedge K_L)] \vee [AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	$LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$
1	I	$K \vee R_n \rightarrow MAR$	$R_n + K + CI \rightarrow R_n$
	II	$K \vee M \rightarrow MAR$	$M + K + CI \rightarrow AT$
	III	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	
2	I	$(AC \wedge K) - 1 + CI \rightarrow R_n$	
	II	$(AC \wedge K) - 1 + CI \rightarrow AT$	(see Note 1)
	III	$(I \wedge K) - 1 + CI \rightarrow AT$	
3	I	$R_n + (AC \wedge K) + CI \rightarrow R_n$	
	II	$M + (AC \wedge K) + CI \rightarrow AT$	
	III	$AT + (I \wedge K) + CI \rightarrow AT$	
4	I	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$	$R_n \wedge (AC \wedge K) \rightarrow R_n$
	II	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$	$M \wedge (AC \wedge K) \rightarrow AT$
	III	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$	$AT \wedge (I \wedge K) \rightarrow AT$
5	I	$CI \vee (R_n \wedge K) \rightarrow CO$	$K \wedge R_n \rightarrow R_n$
	II	$CI \vee (M \wedge K) \rightarrow CO$	$K \wedge M \rightarrow AT$
	III	$CI \vee (AT \wedge K) \rightarrow CO$	$K \wedge AT \rightarrow AT$
6	I	$CI \vee (AC \wedge K) \rightarrow CO$	$R_n \vee (AC \wedge K) \rightarrow R_n$
	II	$CI \vee (AC \wedge K) \rightarrow CO$	$M \vee (AC \wedge K) \rightarrow AT$
	III	$CI \vee (I \wedge K) \rightarrow CO$	$AT \vee (I \wedge K) \rightarrow AT$
7	I	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$	$R_n \,\overline{\oplus}\, (AC \wedge K) \rightarrow R_n$
	II	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$	$M \,\overline{\oplus}\, (AC \wedge K) \rightarrow AT$
	III	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$	$AT \,\overline{\oplus}\, (I \wedge K) \rightarrow AT$

NOTE:

1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

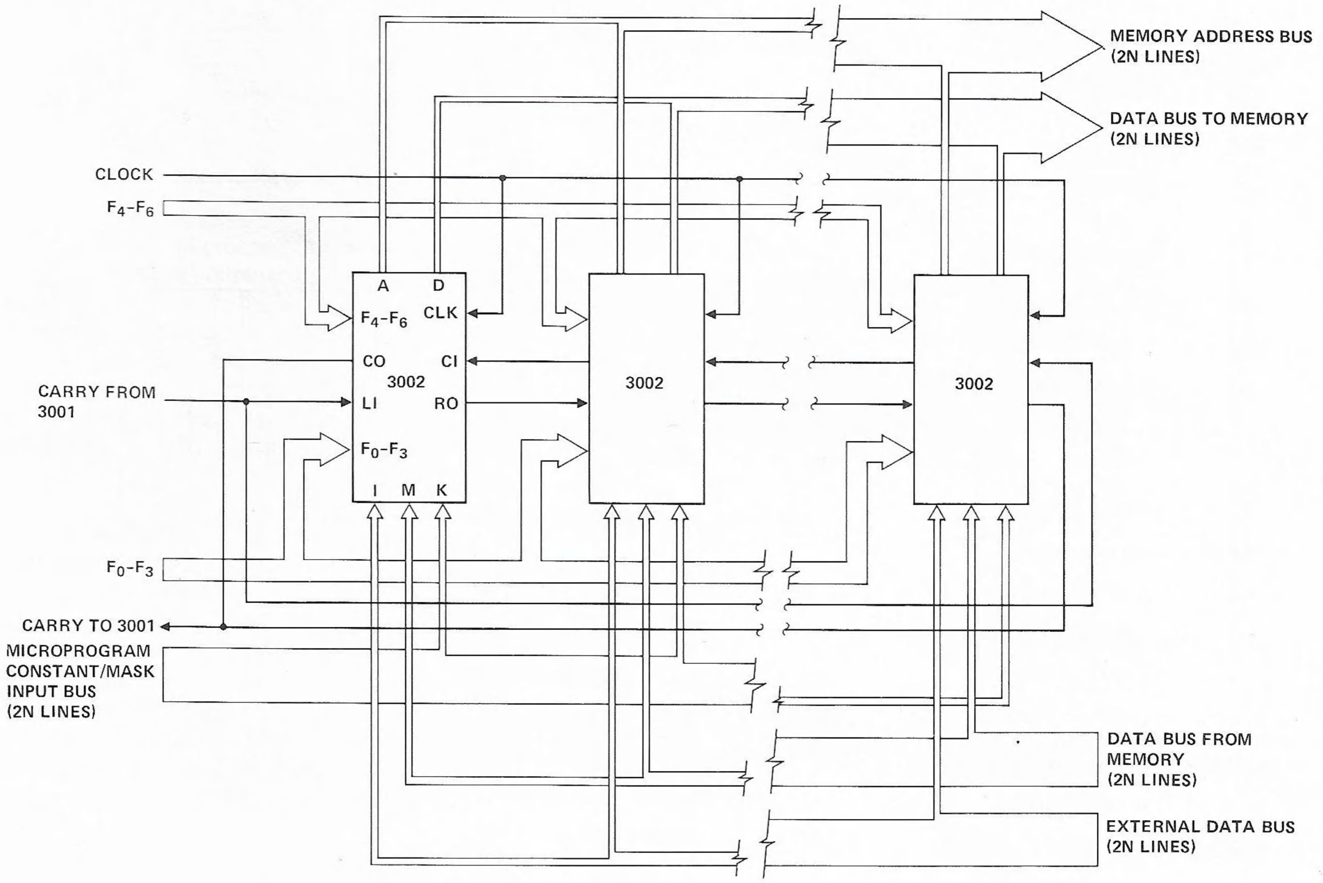
SYMBOL	MEANING
I, K, M	Data on the I, K, and M busses, respectively
CI, LI	Data on the carry input and left input, respectively
CO, RO	Data on the carry output and right output, respectively
R_n	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L, H	As subscripts, designate low and high order bit, respectively
+	2's complement addition
—	2's complement subtraction
$\wedge$	Logical AND
$\vee$	Logical OR
$\overline{\oplus}$	Exclusive-NOR
→	Deposit into

APPENDIX C ALL-ZERO AND ALL-ONE K-BUS MICRO-FUNCTIONS

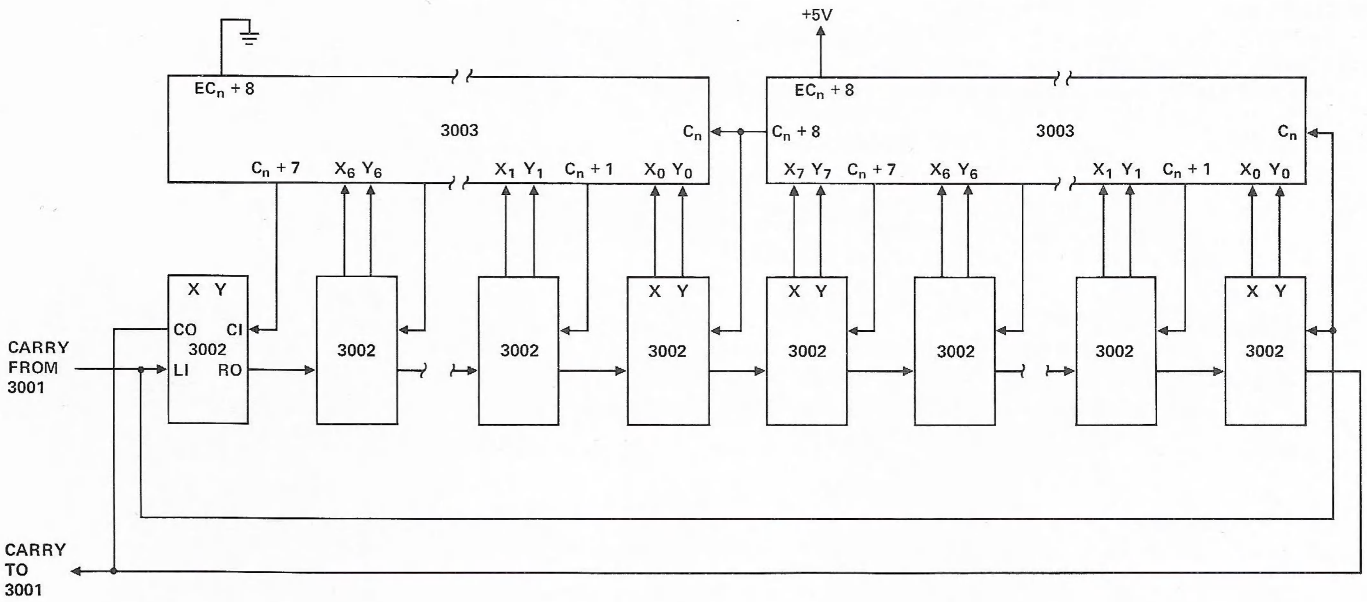
K-BUS = 00 MICRO-FUNCTION		MNEMONIC	K-BUS = 11 MICRO-FUNCTION		MNEMONIC
$R_n + CI \rightarrow R_n, AC$		ILR	$AC + R_n + CI \rightarrow R_n, AC$		ALR
$M + CI \rightarrow AT$		ACM	$M + AC + CI \rightarrow AT$		AMA
$AT_L \rightarrow RO$	$AT_H \rightarrow AT_L$ $\quad LI \rightarrow AT_H$	SRA	(See Appendix B)		–
$R_n \rightarrow MAR$	$R_n + CI \rightarrow R_n$	LMI	$11 \rightarrow MAR$	$R_n - 1 + CI \rightarrow R_n$	DSM
$M \rightarrow MAR$	$M + CI \rightarrow AT$	LMM	$11 \rightarrow MAR$	$M - 1 + CI \rightarrow AT$	LDM
$\overline{AT} + CI \rightarrow AT$		CIA	$AT - 1 + CI \rightarrow AT$		DCA
$CI - 1 \rightarrow R_n$	See Note 1	CSR	$AC - 1 + CI \rightarrow R_n$	See Note 1	SDR
$CI - 1 \rightarrow AT$		CSA	$AC - 1 + CI \rightarrow AT$		SDA
(See CSA above)		–	$I - 1 + CI \rightarrow AT$		LDI
$R_n + CI \rightarrow R_n$		INR	$AC + R_n + CI \rightarrow R_n$		ADR
(See ACM above)		–	(See AMA above)		–
$AT + CI \rightarrow AT$		INA	$I + AT + CI \rightarrow AT$		AIA
$CI \rightarrow CO$	$0 \rightarrow R_n$	CLR	$CI \vee (R_n \wedge AC) \rightarrow CO$	$R_n \wedge AC \rightarrow R_n$	ANR
$CI \rightarrow CO$	$0 \rightarrow AT$	CLA	$CI \vee (M \wedge AC) \rightarrow CO$	$M \wedge AC \rightarrow AT$	ANM
(See CLA above)		–	$CI \vee (AT \wedge I) \rightarrow CO$	$AT \wedge I \rightarrow AT$	ANI
(See CLR above)		–	$CI \vee R_n \rightarrow CO$	$R_n \rightarrow R_n$	TZR
(See CLA above)		–	$CI \vee M \rightarrow CO$	$M \rightarrow AT$	LTM
(See CLA above)		–	$CI \vee AT \rightarrow CO$	$AT \rightarrow AT$	TZA
$CI \rightarrow CO$	$R_n \rightarrow R_n$	NOP	$CI \vee AC \rightarrow CO$	$R_n \vee AC \rightarrow R_n$	ORR
$CI \rightarrow CO$	$M \rightarrow AT$	LMF	$CI \vee AC \rightarrow CO$	$M \vee AC \rightarrow AT$	ORM
(See NOP above)		–	$CI \vee I \rightarrow CO$	$I \vee AT \rightarrow AT$	ORI
$CI \rightarrow CO$	$\overline{R_n} \rightarrow R_n$	CMR	$CI \vee (R_n \quad AC) \rightarrow CO$	$R_n \overline{\oplus} AC \rightarrow R_n$	XNR
$CI \rightarrow CO$	$\overline{M} \rightarrow AT$	LCM	$CI \vee (M \quad AC) \rightarrow CO$	$M \overline{\oplus} AC \rightarrow AT$	XNM
$CI \rightarrow CO$	$\overline{AT} \rightarrow AT$	CMA	$CI \vee (AT \quad I) \rightarrow CO$	$I \overline{\oplus} AT \rightarrow AT$	XNI

NOTE:

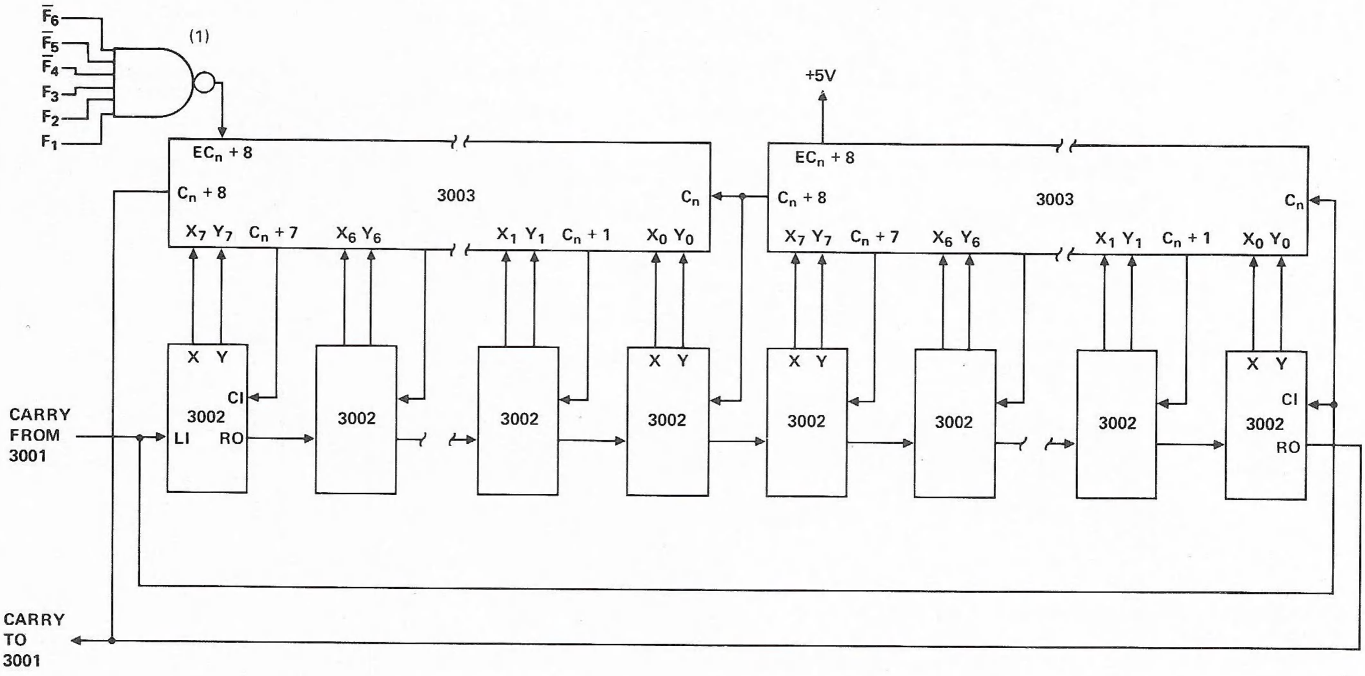
1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.


MEMORY ADDRESS BUS (2N LINES)
DATA BUS TO MEMORY (2N LINES)
CLOCK
F_4-F_6
A
D
F_4-F_6
CLK
CO
CI
3002
LI
RO
F_0-F_3
I
M
K
3002
3002
CARRY FROM 3001
F_0-F_3
CARRY TO 3001
MICROPROGRAM CONSTANT/MASK INPUT BUS (2N LINES)
DATA BUS FROM MEMORY (2N LINES)
EXTERNAL DATA BUS (2N LINES)

Ripple-Carry Configuration
(N 3002 CPE's)



Carry Look-Ahead Configuration
With Ripple Through the Left Slice
(32 Bit Array)



Carry Look-Ahead Configuration
With No Carry Ripple Through the Last Slice
(32 Bit Array)

NOTE:
(1) A bit from microprogram memory can be used to replace the gate shown above and inform the 3003 of an active Shift Right operation.

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Suite 178
Dallas, Texas 75240
Tel: (214) 661-8829
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Great Lakes Region:
856 Union Road
Englewood, Ohio 45322
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NOTE: This is a preliminary specification and is subject to revision without notice.

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